IN THE SPECIFICATION

1. Please amend paragraph [0001] on page 1 of the application as follows:

[0001] The present invention is related to those disclosed in:

1) United States Patent Application Serial No. 10/630,322 ~~[Docket No. NATI15-05644]~~, filed concurrently herewith, entitled "CIRCUITS FOR REDUCING LEAKAGE CURRENTS IN PULL-UP AND PULL-DOWN CIRCUITS USING VERY SMALL MOSFET DEVICES;" and

2) United States Patent Application Serial No. 10/630,311 ~~[Docket No. NATI15-00037]~~, filed concurrently herewith, entitled "CIRCUITRY FOR REDUCING LEAKAGE CURRENTS IN A PRE-CHARGE CIRCUIT USING VERY SMALL MOSFET DEVICES."

2. Please amend paragraph [0002] on page 1 of the application as follows:

[0002] Patent Application Serial Nos. 10/630,322 ~~[Docket No. NATI15-05644]~~ and 10/630,311 ~~[Docket No. NATI15-00037]~~ are commonly assigned to the assignee of the present invention. The disclosures of the related patent applications are hereby incorporated by reference for all purposes as if fully set forth herein.

3. Please amend paragraph [0025] on page 10 of the application as follows:

[0025] FIGURE 1 illustrates exemplary phase-locked loop (PLL) 100, which incorporates commonly used analog switches in which MOSFET sub-threshold leakage currents are reduced according to the principles of the present invention. PLL 100 comprises frequency divider 110, phase-frequency detector 120, charge pump and loop filter circuit 130, voltage controlled oscillator 140 and frequency divider [[160]] 150. Frequency divider 110 divides the frequency of the input signal, VIN, by R, where R may be an integer of a fractional value. Frequency divider 150 divides the frequency of the output signal, VOUT, by N, where N may be an integer or a fractional value.

4. Please amend paragraph [0045] on pages 18-19 of the application as follows:

[0045] Unfortunately, pre-charge circuit 400 experiences high leakage current when pre-charge circuit 400 is disabled. When Pre-Charge=0, P-channel transistor 423 is off, but P-channel transistor [[423]] 424 is still on. Thus, the VMID node sits at approximately 0 volts. Since Pre-charge=0 is coupled to the gate of N-channel transistor 431 and VMID=0 is coupled to the source of N-channel transistor 431, the Vgs of N-channel transistor 431 is approximately 0 volts. This permits sub-threshold leakage currents in small-feature-sized processes. Therefore, a leakage current path forms between the high impedance node, VC, and the VSS rail (i.e., ground) through N-channel transistor 431 and P-channel transistor 424.